AND8316

3.3 V / 20 A Post-Regulator Driven by the NCP4331

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INTRODUCTION

In applications where several output voltages must be tightly regulated, so−called Secondary Side Post Regulators (SSPR) are generally ideal solutions.

Practically, as explained in application note AND8314 [1]:

- A main power supply generates one or several outputs. One of them is monitored and traditionally regulated by the regulation means of this main converter. The converter duty ratio is modulated accordingly.
- SSPRs post−regulate the remaining outputs, ***by directly drawing the energy from the transformer secondary ac voltage*.**

As of today, magnetic amplifier post−regulators (mag amp) are very popular for ATX applications (desktop PFC power supplies). However, they are the seat of important conduction losses that limit their interest in the raging struggle for energy savings.

NCP4331−driven post−regulators represent a major leap towards efficiency. Like mag amp, they can be viewed as buck converters with the ability to operate from a pulsed input voltage. However, NCP4331 driven post−regulators dramatically improves the efficiency of the power processing since:

- They significantly reduce the conduction losses as the mag amp saturable coil is removed and the diodes are replaced by low $R_{DS(on)}$ N−MOSFETs (synchronous rectification)
- The switching losses are minimized since a smart sequencing ***softens*** three out of the four switching transitions of the MOSFETs.

Application note AND8314 [1] proposes a systematic process to design NCP4331 driven post−regulators. As an example, a 3.3 V / 20 A board has been built and has been coupled to a 2−switch forward converter (Note 1) for testing. The objective of this paper is to present this board and to report its main performance.

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1. One can associate the NCP4331 to several architectures (like forward, active clamp forward or half bridge converters). As a matter of fact, any converter able to provide the NCP4331 post−regulator with a square wave source can use this concept, as long as the NCP4331 maximum ratings are not exceeded (in particular, the “BST” and “HB” 40 V maximum ratings)

The Board

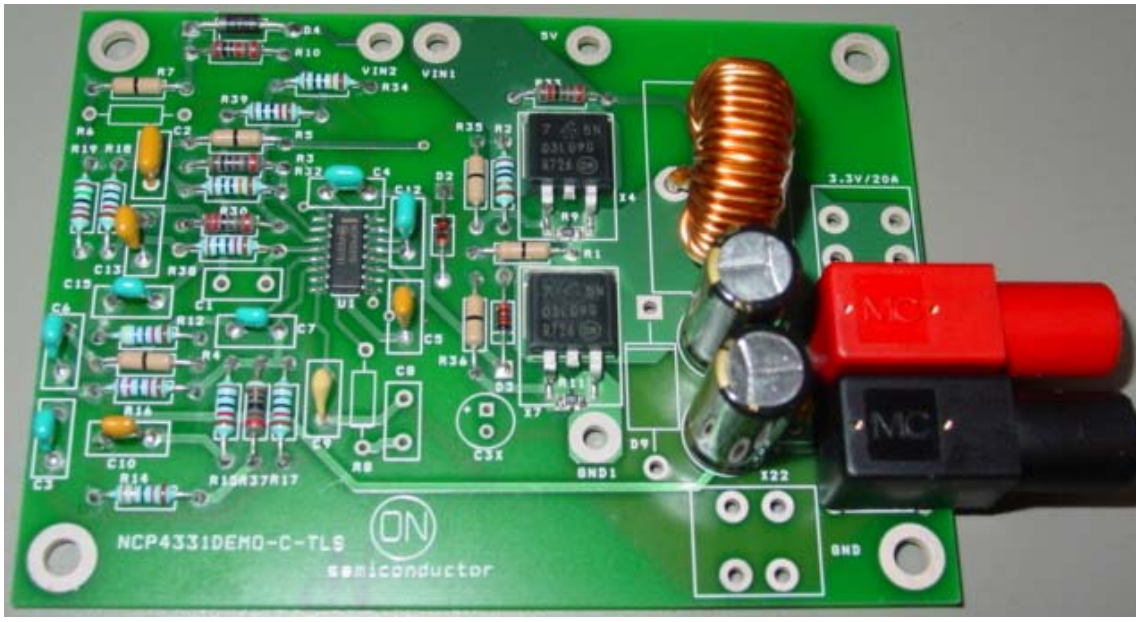


Figure 1. 3.3 V / 20 A Post−regulator

Application Schematic

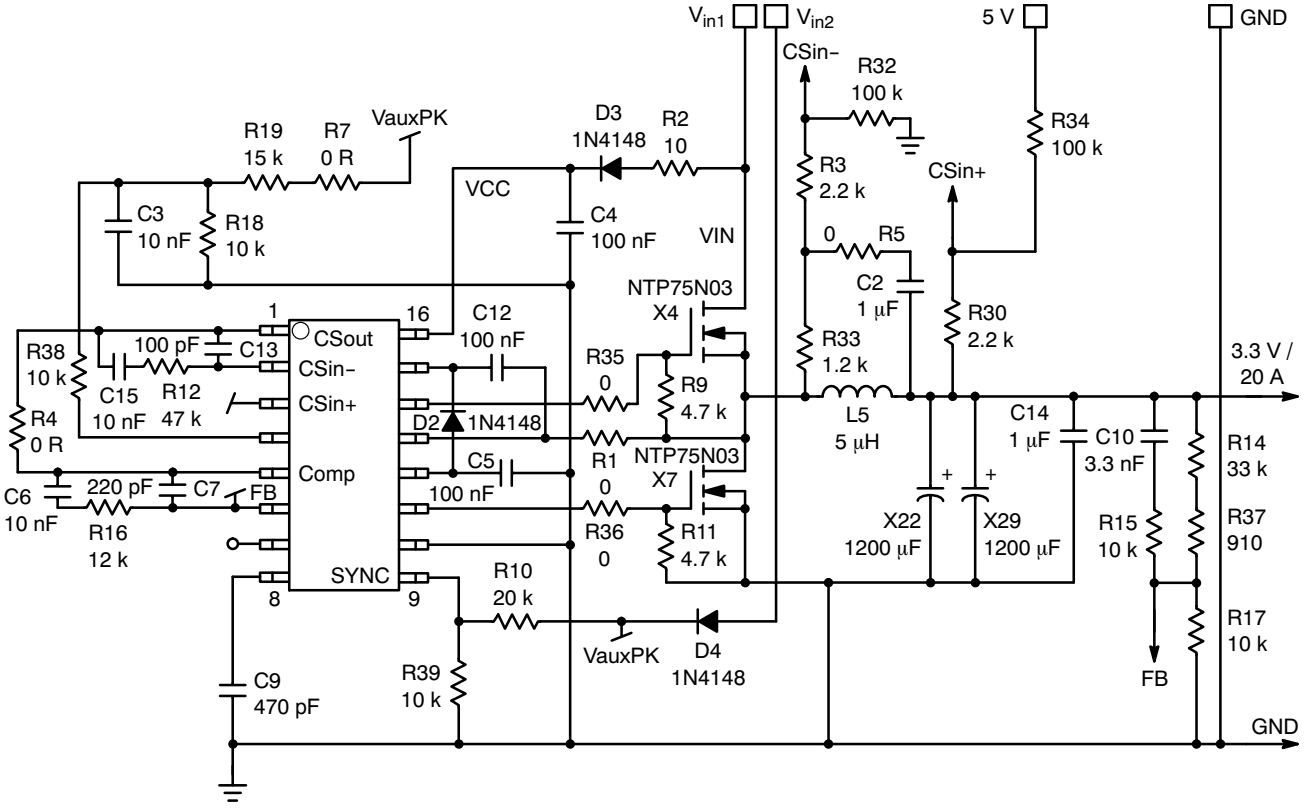


Figure 1. Application Schematic

PCB Layout

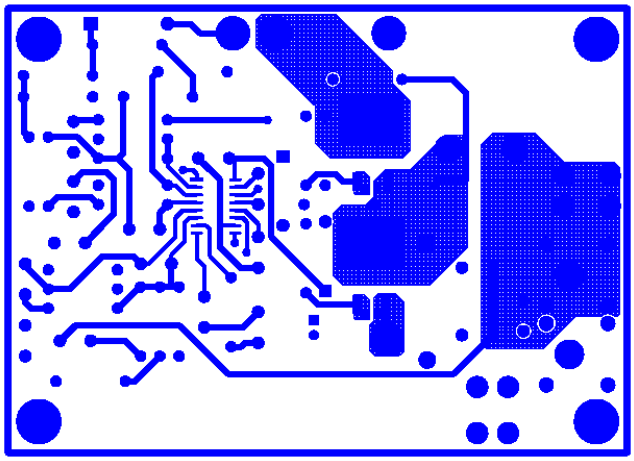


Figure 2. PCB Layout (Top Side)

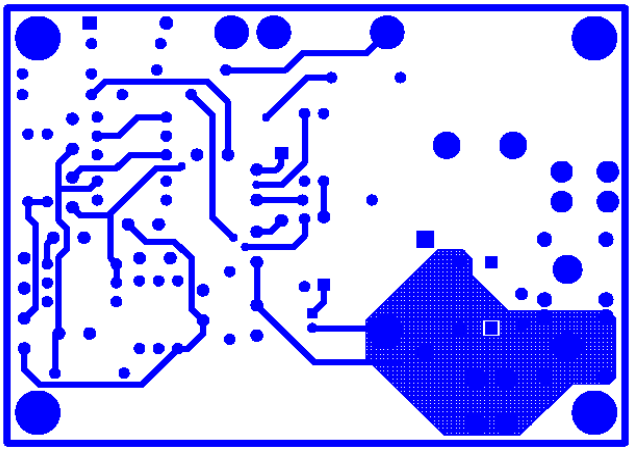


Figure 3. PCB Layout (Bottom Side)

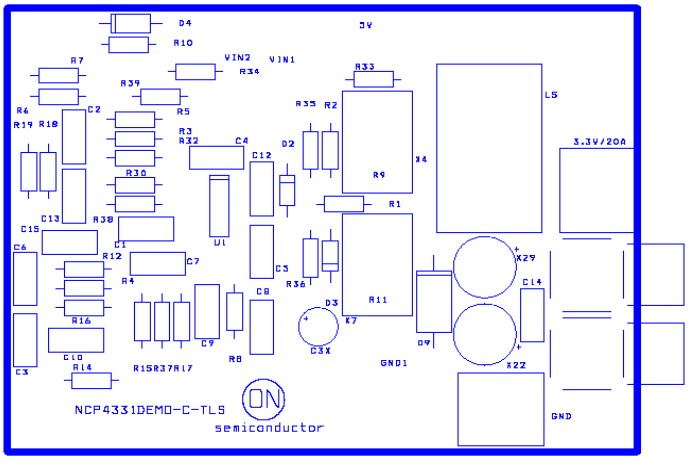


Figure 4. Component Placement

Test Conditions

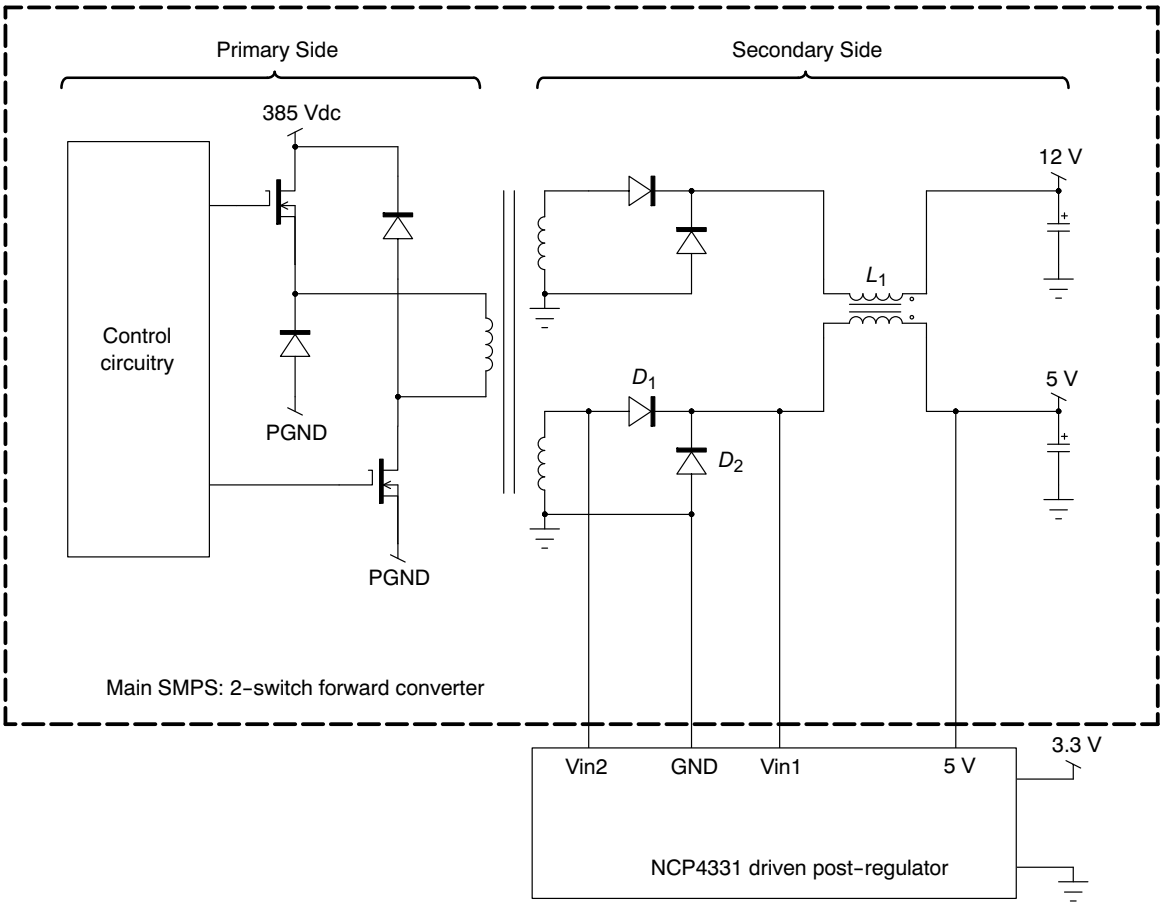


Figure 5. Test Conditions

When plugging the NCP4331 board to a main converter, there are maximum ratings not to exceed. In particular, the V_{in1} and V_{in2} voltages must remain below 30 V, possible spikes included. As for the negative voltage of V_{in2}, it should not exceed the permissible reverse voltage of diode D4 that is 75 V.

The NCP4331 board (post−regulator) is coupled to a 2−switch forward converter (main SMPS).

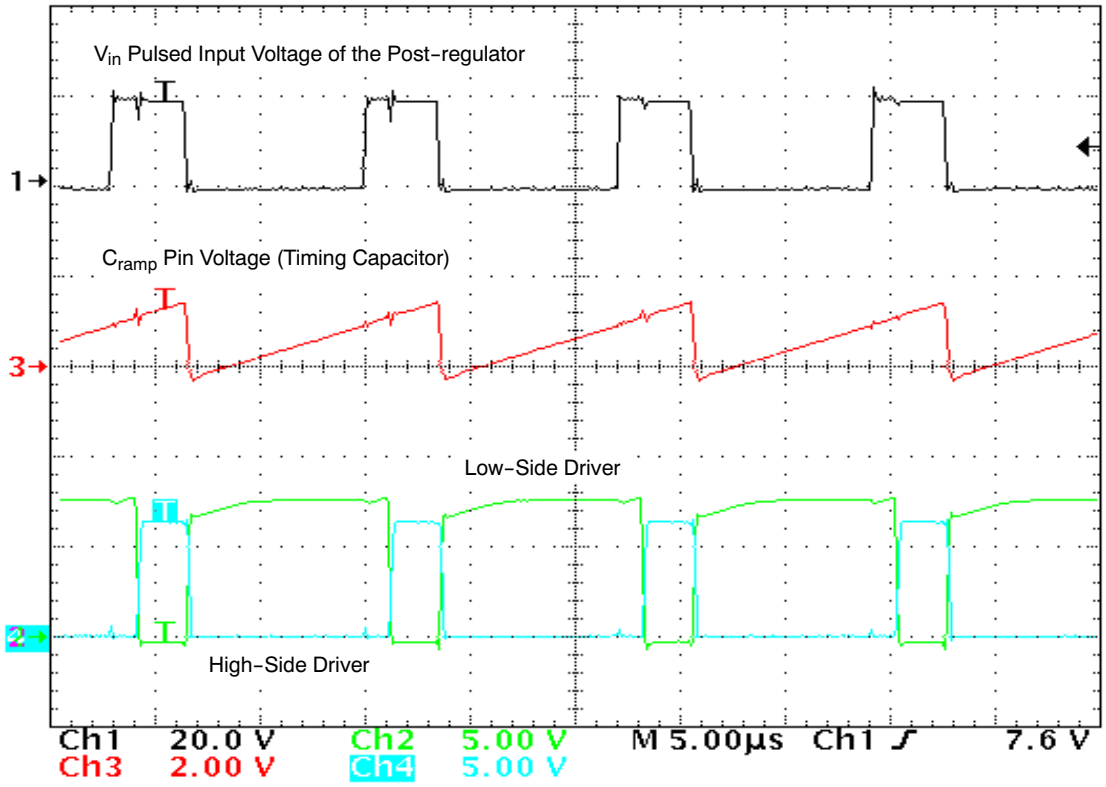
The post−regulator receives four signals from the main SMPS:

- V_{in1}: this is the pulsed input voltage of the post−regulator. Practically, V_{in1} results from the rectification of the secondary winding voltage that feeds the 5 V output. In our case, two diodes D_1 and D_2 performs the rectification function. One of them or both could be replaced by synchronous rectifiers but if it was the case, still V_{in1} should be the rectified voltage.
- V_{in2}: this voltage is used for synchronization and for the under−voltage protection (UVP). Another option could be to re−use V_{in1}. However, as explained in [1], V_{in2} immediately drops to zero when the main SMPS stops operating (Note 2). Thus, using V_{in2}, the UVP can disable the post−regulator without delay at that moment. Also, V_{in2} is generally cleaner than V_{in1}.
- GND: common ground for the secondary side of the main SMPS and for the post−regulator
- 5 V: this voltage can be used to set the maximum permissible level for the load current when the current loop is implemented for CCCV operation. Any other available voltage could be used as well. However, using 5 V helps the 3.3 V output track the 5 V one since the current threshold increases as a function of the 5 V voltage.

2. This is not necessarily the case with V_{in1} that can remain in the range of the 5 V voltage due to the connection by L_1.

Steady State Operation

1. General Behavior – Typical Waveforms



Conditions: 5 A load on the 12 V, on the 5 V and on the 3.3 V outputs

Figure 6. Main Waveforms

2. Output Regulation and Ripple

The 3.3 V voltage and its ripple were measured at different load levels. A 5 A load was applied to the two main output (12 V and the 5 V).

I_{out}	(A)	0	5	10	15	20
V_{out}	(V)	3.321	3.320	3.318	3.317	3.316
$(\Delta V_{out})_{pk-pk}$	(mV)	60	60	60	60	60

The output voltage is very stable on the load range and the peak to peak ripple is very low.

Regarding the peak to peak ripple, the performance is even better than that computed than in AND8314 because:

- The board embeds output capacitors that exhibit a lower ESR. Practically, 1200 µF / 10 V FM series Panasonic capacitors are used instead of 1200 µF / 6.3 V leading to a global ESR of about 9 mΩ instead of 13 mΩ at 20°C
- The switching frequency of the 2−switch forward is 82 kHz while the AND8314 computations are based on a 70 kHz switching frequency.

Thermal Measurements

The following results were obtained using a thermal camera, after a 2 h operation at 25°C ambient temperature and full load. These data are indicative.

High−side Power MOSFET	Low−side Power MOSFET	Bulk Capacitor	Output Inductor	Controller
95°C	100°C	60°C	105°C	65°C

Measurements Conditions:

- Plateau level of the input voltage: 19 V
- Load current: 19 A
- Open frame, no fan

No Load Operation

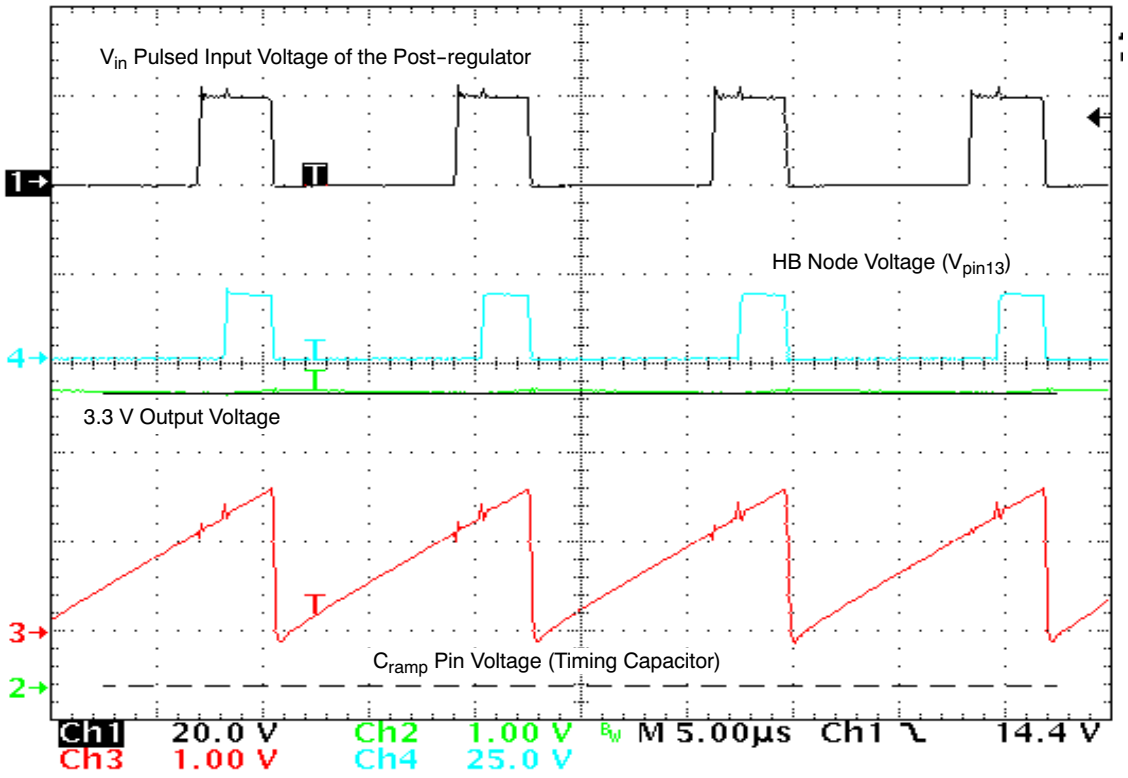


Figure 7. Main Waveforms in No Load

In light load, the NCP4331 keeps operating in continuous conduction mode.

This has two advantages:

- The output voltage remains accurately regulated in no load
- The function transfer is not modified in light load (as it would if the system entered discontinuous conduction mode) and there is no discontinuity in the operation. The dynamic performance stay similar to that obtained in nominal load conditions.

Dynamic Performance

Tests are made to check the dynamic performance under sharp load variations.

More specifically, the output voltage deviation is observed when the 6 A step load is applied. This is performed in two cases:

- The load current jumping from 14 A to 20 A and vice versa.
- The load swinging between 0 and 6 A.
- Slew rate: 80 A/ms (in both cases).

In the following plots, the 3.3 V output voltage is observed with a 3.320 V offset. In other words, trace 2 is referenced to its nominal level instead of ground for an eased observation of the deviation.

As testified by the following plots, in the two studied cases, the output voltage deviation is very limited and remains within a 100 mV range.

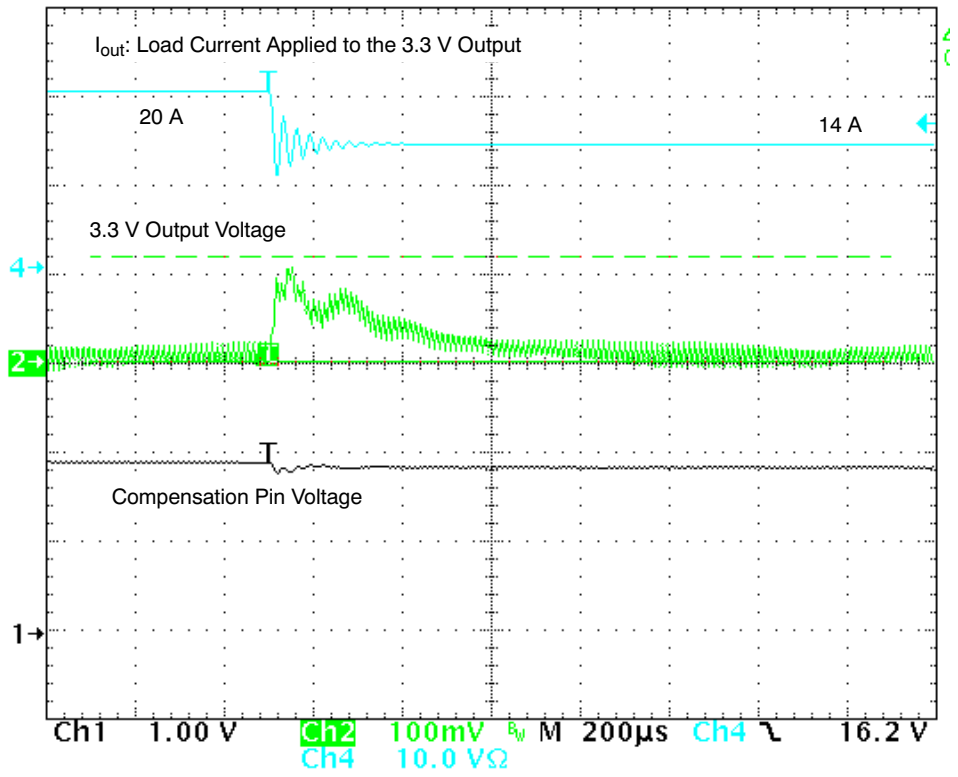


Figure 8. I_{out} Falling from 20 A to 14 A

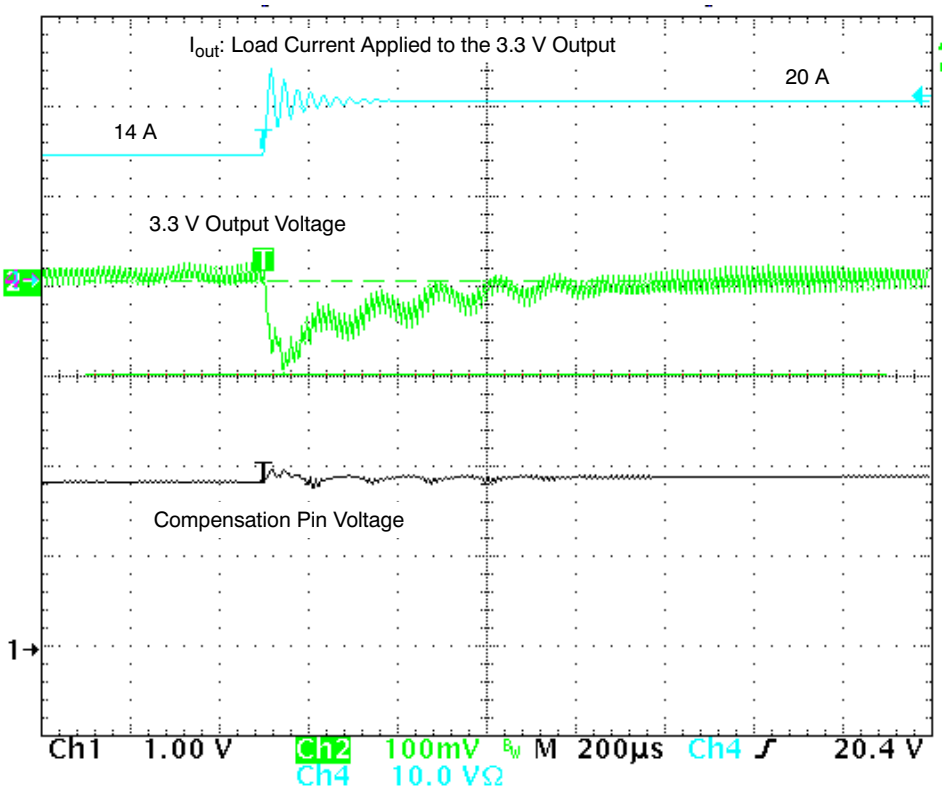


Figure 9. I_{out} Rising from 14 A to 20 A

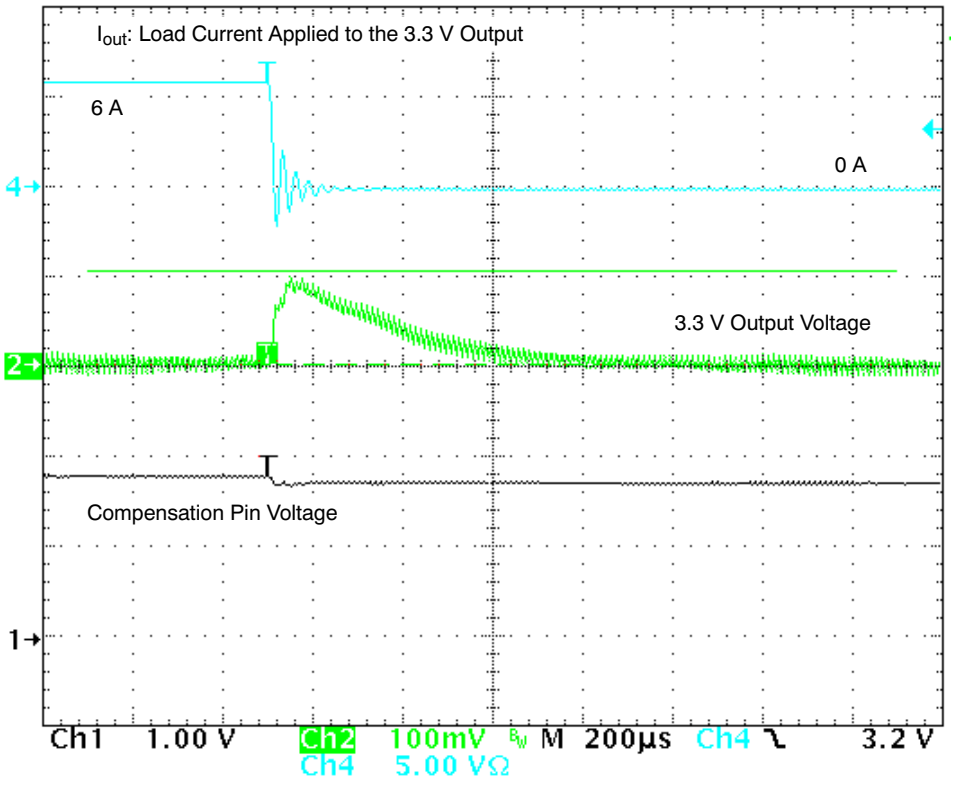


Figure 10. I_{out} Falling from 6 A to 0 A

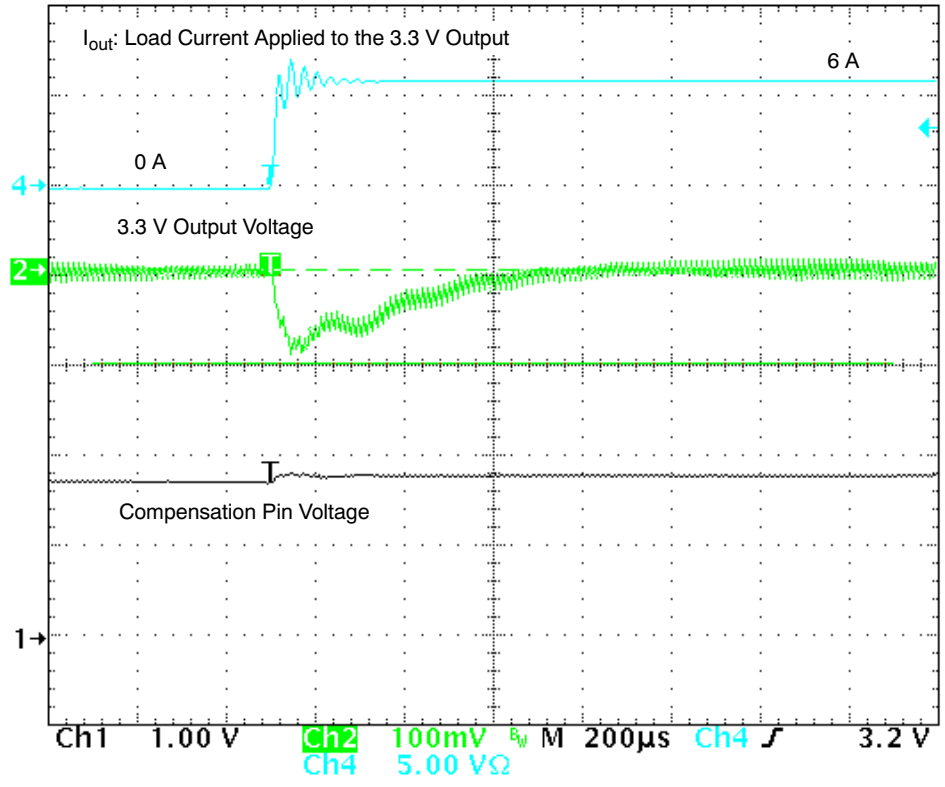


Figure 11. I_{out} Rising from 0 A to 6 A

Current Limitation

As explained in [1], the NCP4331 allows Constant Current Constant Voltage operation (CCCV). For this, the output of the current loop error amplifier (pin 1) can be directly connected to the output of the voltage loop error amplifier (pin 5).

As proposed and detailed in AND8314 (reference [1]), the demo−board uses the series resistor of the coil to sense the current. Such a solution saves the additional losses that a specific current sensing resistor would generate and avoids the complexity and cost inherent to a solution based on current sense transformers.

The following figure portrays the current sensing solution based on the coil series resistor. The 5 V output is used to set the level at which the current loop clamps the inductor current according to the following equation:

$$I_{out,max} = \frac{\frac{R_{30} \cdot 5\ V}{R_{34}}}{r_L} \quad \text{(eq. 1)}$$

Where:
r_L is the inductor series resistor
$I_{out,max}$ is the maximum load current
5 V is the 5 V voltage.

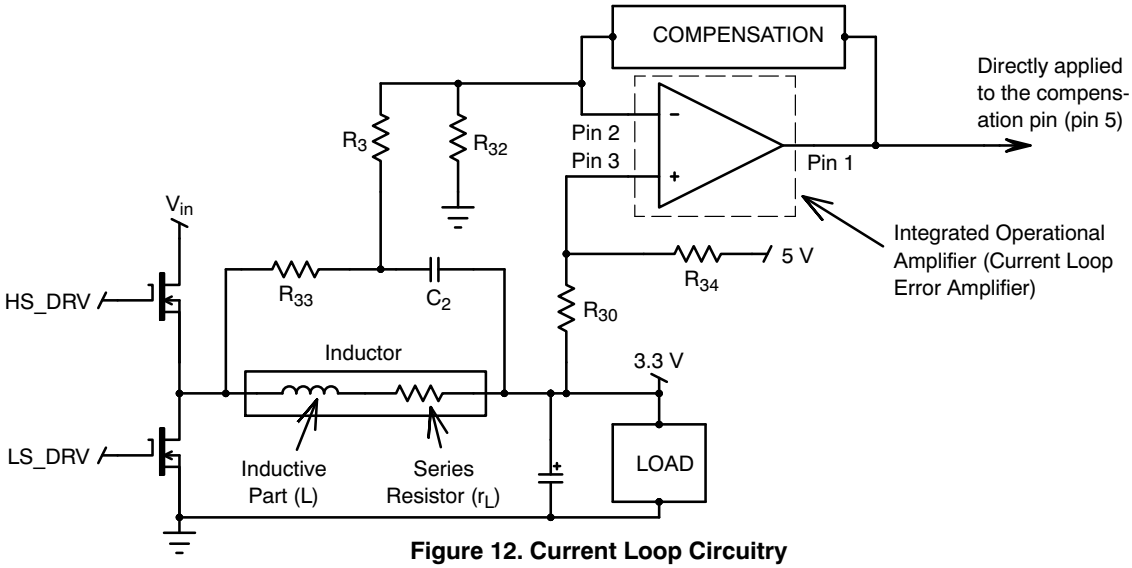


Figure 12. Current Loop Circuitry

The current loop error amplifier must properly be compensated. In the demo−board, the crossover frequency is rather high and hence, it tends to activate the current loop a bit earlier than expected by making it sensitive to the output current ripple. That is why the over current threshold is in the range of 22 A instead of 27 A. For a more precise current limitation, the crossover frequency can be reduced by diminishing the R_{12} resistor to 10 kΩ for instance (in order to increase the frequency of the associated zero). More generally, it is recommended to set a relatively low crossover frequency (one fifth of the switching frequency or lower) by following the AND8314 design procedure.

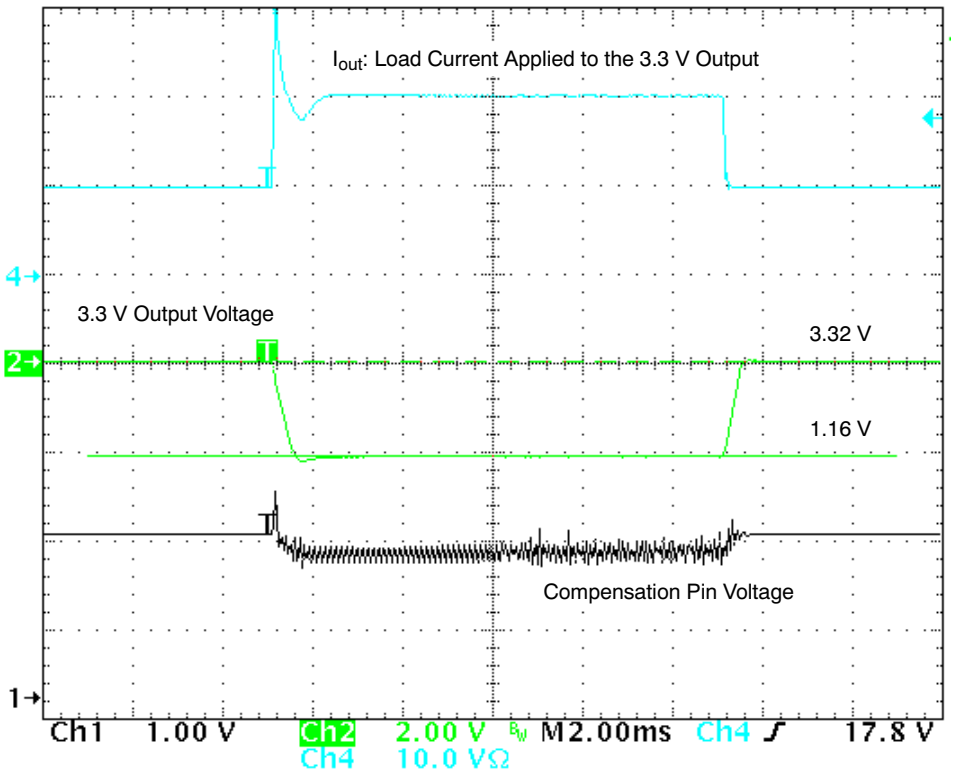


Figure 13. CCCV Operation (Load Current Varying between 10 and 30 A)

As expected, when the load current exceeds the allowed level, the output voltage is reduced so that the permissible level (21 A) is no more exceeded. In the test condition, when the load demand is excessive (30 A), the output voltage drops to about 1.16 V and stabilizes at this level. This is because under this voltage, the electronic load used for this test cannot draw more than the 21 A permissible level.

When the load current drops to a normal level (10 A here), the output voltage recovers its 3.3 V nominal value.

Remarks:

In our application, the following components are used for the current loop:

- R_3, R_{32}, R_{33} and C_2 to sense the current
- R_{30} and R_{34} to set the current threshold
- R_{12}, C_{13} and C_{15} to compensate the loop

- The current loop has some soft−start effect since the coil current is limited during the start−up sequence. That is why the soft−start facility is not used in our application (pin 7 open).
- **Since the NCP4331 is able to control the current by monitoring the coil voltage, one can protect the post−regulator in case of output short−circuit or over load, without implementing any specific current sense resistor that would lead to additional losses and hence, degrade the efficiency**.
- If the current loop is not necessary, just ground pins 1 to 3.

Start−up Sequences

Start−up sequences are performed by abruptly enabling the main SMPS (by applying a V_{cc} voltage to its controller). The load conditions are:

- 10 A on the 12 V output
- 10 A on the 5 V output
- 10 A (Figure 14) and 0 A (Figure 15) on the 3.3 V output.

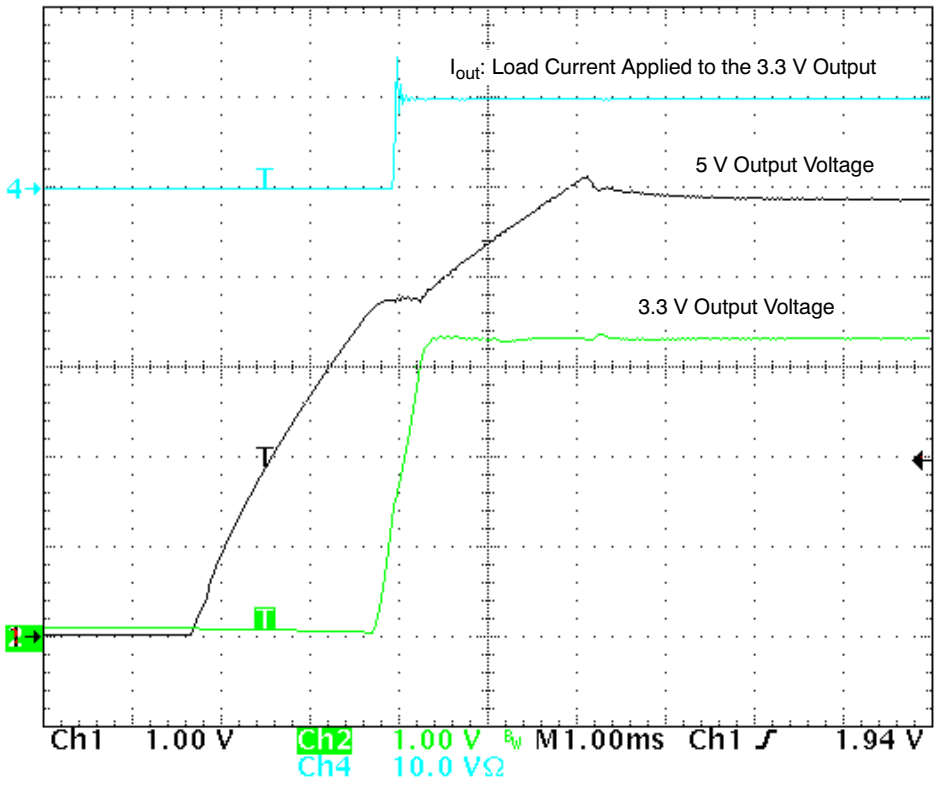


Figure 14. Start−up Sequence with 5 A Load on the 3.3 V Output

In both situations (5 A on the 3.3 V − Figure 14 − and in no load − Figure 15), The 3.3 V voltage rise is monotonic. The delay between the 5 V and the 3.3 V rise is controlled by the Under−Voltage Protection. Practically, the pin4 voltage must exceed 2 V for operation otherwise the circuit is disabled. In our application, pin4 receives a filtered portion of the synchronization signal. The delay between the 5 V and the 3.3 V occurrence is then dependent of the pin 4 filtering time constant and in particular on the capacitor C_3 of the application schematic (see Figure 2).

If you need to meet specific needs, please refer to the appendix of this application note that shows how to accurately control the start−up phases.

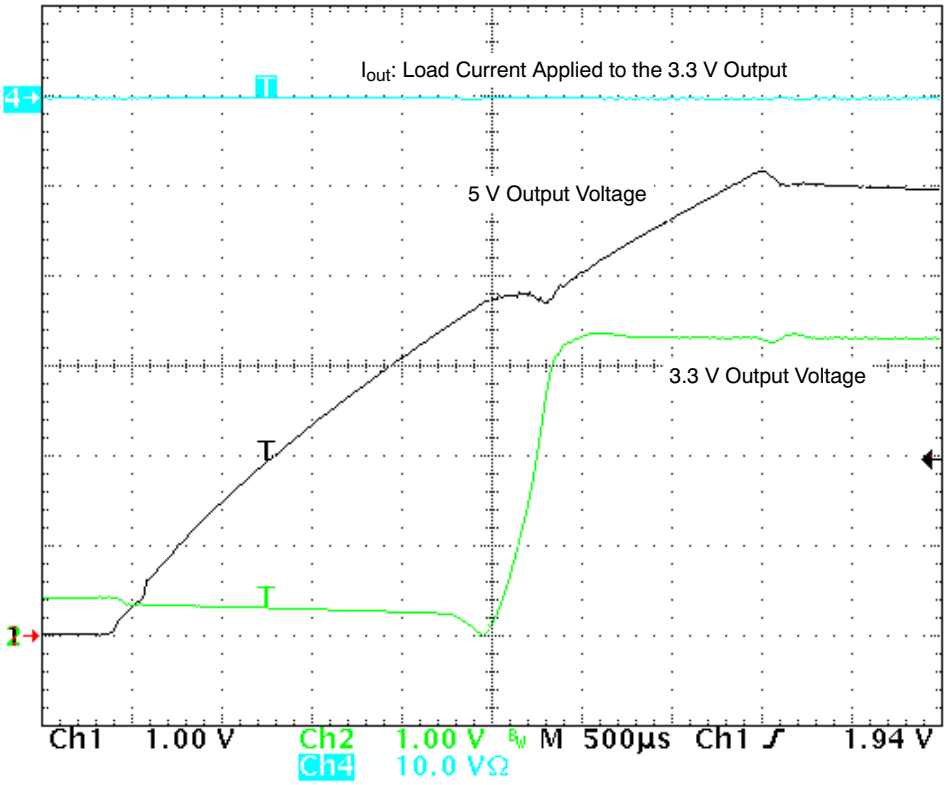


Figure 15. Start−up Sequence (No Load on the 3.3 V Output)

Stop Sequences

Stop sequences are performed by abruptly disabling the main SMPS (by stopping feeding its controller). The load conditions are:

- 10 A on the 12 V output
- 10 A on the 5 V output
- 10 A (Figure 16) and 0 A (Figure 17) on the 3.3 V output.

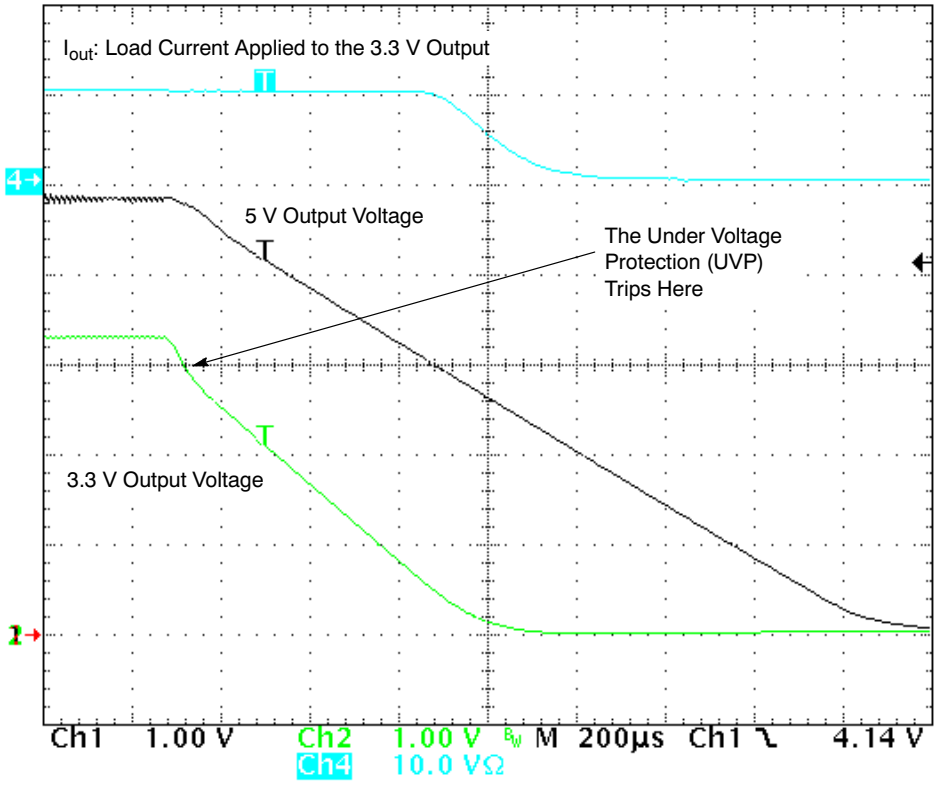


Figure 16. Stop Sequence with 5 A Load on the 3.3 V Output

In both situations (5 A on the 3.3 V – Figure 14 – and in no load – Figure 15), the 3.3 V voltage decay is monotonic. Also, the 3.3 V and the 5 V voltages start to drop simultaneously.

We can note two falling slopes in Figure 16:

- For about the first 50 µs of the decay, the slope is steep. This is because the absence synchronization pulses forces the post−regulator in a free−wheeling sequence that sharply discharges the output capacitor. This short phase stops when the NCP4331 Under−Voltage Protection (UVP) detects the absence of input voltages and disables the NCP4331.
- For the second phase, the NCP4331 is off and the 3.3 V is simply discharged by the 5 A load.

In no load condition (Figure 17) there is a third phase. More specifically:

- Again, in the first 50 µs of the decay, the post−regulator is forced in free−wheeling, which leads to a sharp decay of the 3.3 V output voltage until the UVP triggers and disables the NCP4331.
- During the second phase, the decay slope is flat unlike what we observe in Figure 16. This is because there is no load, and hence only some leakage discharges the output.
- The third phase (additional phase) starts when the 5 V voltage goes below the 3.3 V one. At that moment, the 5 V load starts to discharge the 3.3 V output through the high−side MOSFET body diode and the coil of the post−regulator and through the 5 V output choke.

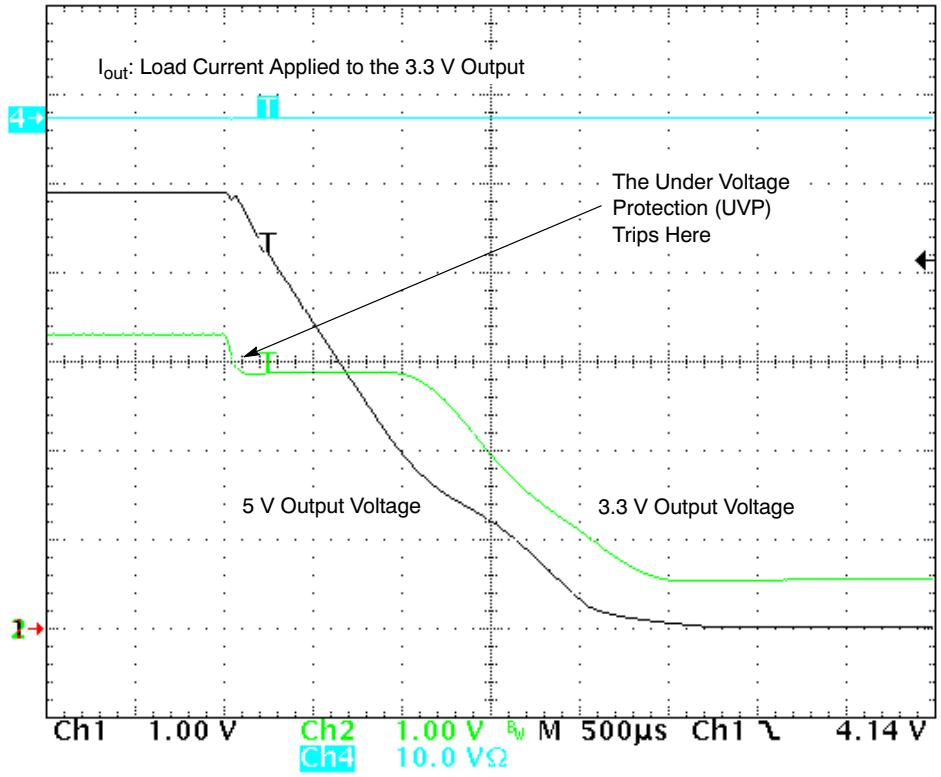


Figure 17. Stop Sequence (No Load on the 3.3 V Output)

Efficiency Data

The post−regulator input power is estimated by averaging the product ($V_{in2} \cdot I_{Vin1}$) where V_{in2} is the voltage across the 5 V auxiliary winding and (I_{Vin1}) is the current absorbed by the V_{in1} terminal of the post−regulator (refer to Figure 5). As necessary, the losses in diode D_1 are then taken into account.

The 12 V is loaded by a 15 A current while the 5 V load is varied between 12 and 20 A so that the total power absorbed by the 3.3 V and 5 V outputs does not exceed 125 W.

Doing so, the efficiency curve of Figure 18 is obtained.

The efficiency is maximum for a 10 A load (89.5%) and is in the range of 86% at full load.

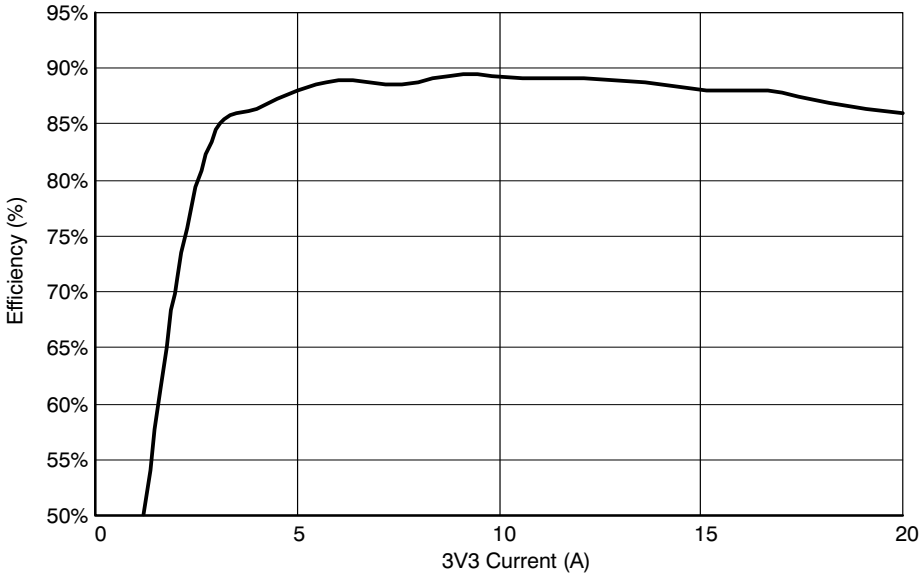


Figure 18. Efficiency of the NCP4331−driven Post−regulator

A comparison is made to a mag amp built as shown by Figure 19. The same output (L, C) filter is implemented for an apple to apple comparison.

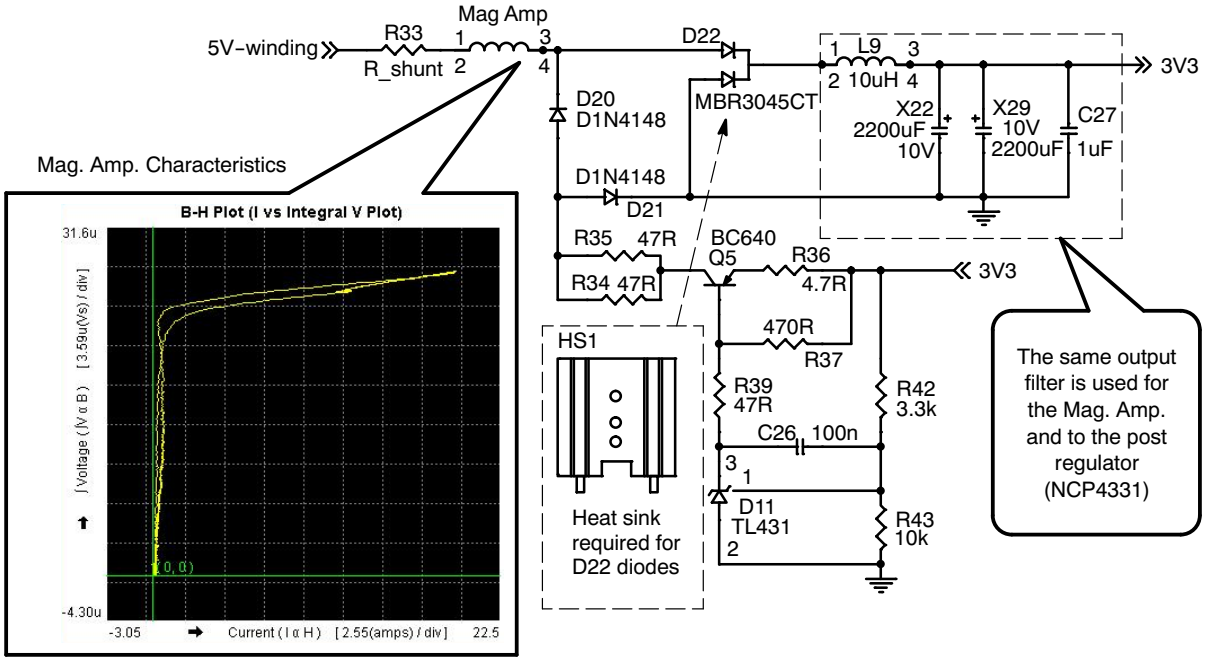


Figure 19. Mag Amp Circuitry

This test shows that the NCP4331 significantly improves the efficiency. As testified by Figure 20, there is a 7% difference between the NCP4331 efficiency and the mag amp one. This difference is relatively stable over the full power range. In our application, this results in a 1.5% increase in the global efficiency of the power supply.

The efficiency improvement can also be quantified as a function of the losses amount that is eliminated by the NCP4331. About 10% of the post−regulator output power is saved thanks to the NCP4331!

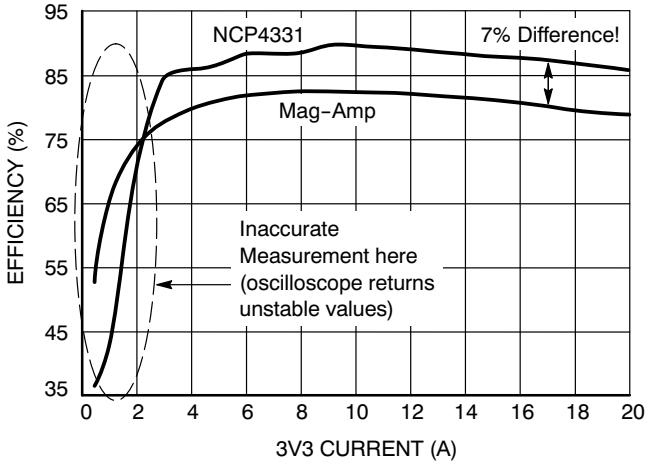


Figure 20. NCP4331 & Mag Amp Efficiency vs. Load Current

Bill Of Materials

Ref Des	Description	Part Number	Manufacturer
C2 / C14	1 μF / 50 V		various
C3, C6, C15	10 nF / 50 V		various
C4, C5, C12	100 nF / 50 V		various
C7	220 pF / 50 V		various
C9	470 pF / 50 V		various
C10	3.3 nF / 50 V		various
C13	100 pF / 50 V		various
R1, R4, R5, R7, R35, R36	Resistor, Axial Lead, 0 Ω, 1/4 W		various
R2	Resistor, Axial Lead, 10 Ω, 1/4 W		various
R3	Resistor, Axial Lead, 1 kΩ, 1/4 W		various
R9, R11	CMS, 1206, 4.7 kΩ, 1/4 W		various
R10	Resistor, Axial Lead, 20 kΩ, 1/4 W		various
R12	Resistor, Axial Lead, 47 kΩ, 1/4 W		various
R14	Resistor, Axial Lead, 33 kΩ, 1/4 W		various
R16	Resistor, Axial Lead, 12 kΩ, 1/4 W		various
R15, R17, R18, R39, R38	Resistor, Axial Lead, 10 kΩ, 1/4 W, 1%		various
R19	Resistor, Axial Lead, 15 kΩ, 1/4 W		various
R30	Resistor, Axial Lead, 2.2 kΩ, 3 W, 1%		various
R32, R34	Resistor, Axial Lead, 100 kΩ, 1/4 W, 1%		various
R33	Resistor, Axial Lead, 1.2 kΩ, 3 W, 1%		various
R37	Resistor, Axial Lead, 910 Ω, 1/4 W, 1%		various
R9	Resistor, Axial Lead, 560 kΩ, 1/4 W, 1%		various
R10	Resistor, Axial Lead, 10 kΩ, 1/4 W, 1%		various
D1, D3, D4	DO−35 diode	1N4148	various
L4	Toroid coil 4.5 μH @ 25 A	86A−7092	Delta Electronics
X4, X7	D^2PAK, 75 A / 30 V Power MOSFET	NTB75N03L09G	ON Semiconductor
X22, X29	1200 μF / 10 V, electrolytic capacitor	EEUFM1A122 (FM series)	Panasonic
	Controller (SOIC−16 version)	NCP4331DR2G	ON Semiconductor

Vendors Contacts

Vendor	Contact	Product Information
Delta Electronics	cliu@delta−europe.com	http://www.delta.com.tw/product/cp/inductor/inductor_main.asp

Conclusion

A post−regulator based on the NCP4331 delivering 3.3 V / 20 A was presented. The board is to be viewed as a daughter board to be associated to a main converter.

As illustrated in this paper, the NCP4331 embeds an error amplifier for an accurate regulation of the output voltage. In addition, it can control the load current (Constant Current Constant Voltage approach − CCCV) without the need for a specific current sense resistor that would lead to extra losses. Also, the circuit functions and in particular the Under−Voltage Protection (UVP) help properly manage the start−up and stop sequences.

Ultimately, thanks to its efficiency and performance, a NCP4331 driven post−regulator must be a solution of choice when designing most multi−output converters like desktop power supplies.

For more information on how to design such a post−regulator, you can refer to application note AND8314 that is available at:

http://www.onsemi.com/pub/Collateral/AND8314−D.PDF

References

[1] AND8314, “Key steps to design a post−regulator driven by the NCP4331”, by Joël Turchi, www.onsemi.com

[2] NCP4331 Data Sheet available at www.onsemi.com

Appendix: Adjusting the Output Voltage Sequencing

Some applications like ATX power supplies, specify very severe constraints. Among them, we can list the following typical ones:

- the rising time of each signal should be between 2 and 20 ms
- the rising and falling slopes should be monotonic

For these stringent requirements, it is recommended to have the post−regulator starting up as soon as possible when the main converter enters operation. If not, we may observe some discontinuity on the main outputs when the NCP4331 post−regulator starts to operate.

To do so, the circuitry for Under−Voltage Protection can be modified as portrayed by Figure 21. Practically, a peak detector replaces the averaging circuitry for an immediate detection of the activity of the main converter.

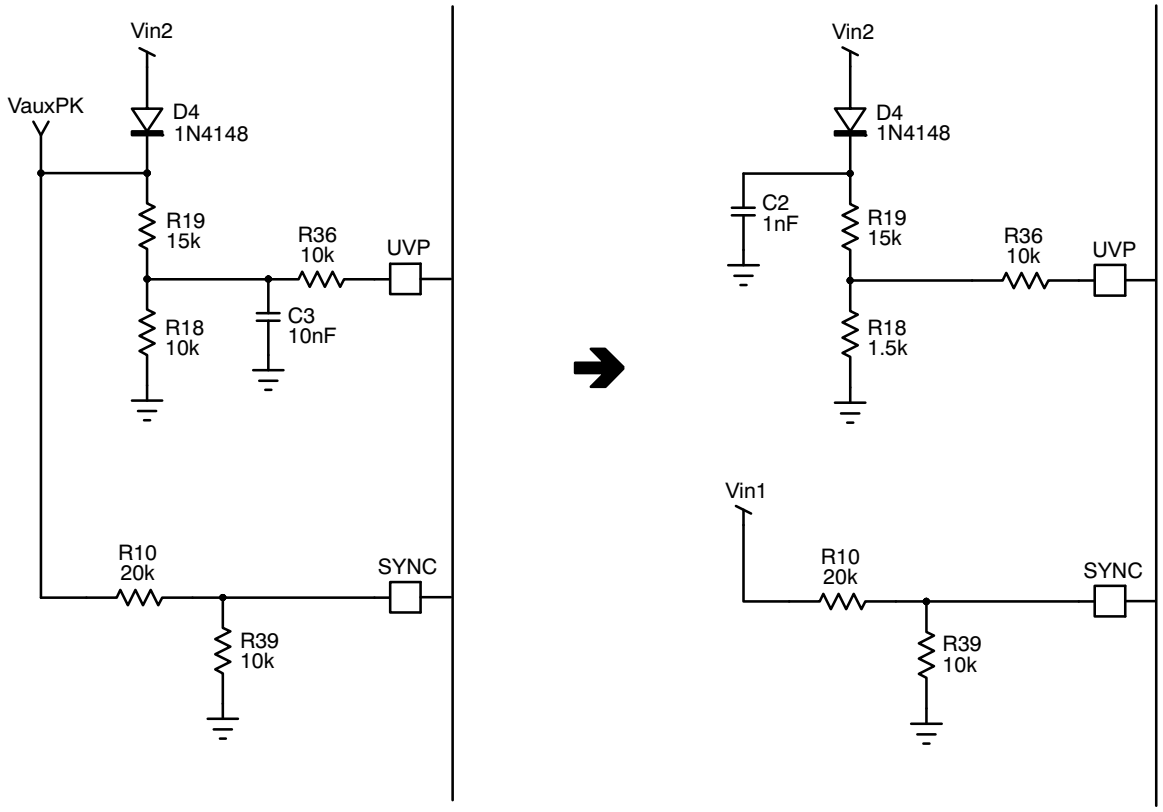


Figure 21. Changes in the UVP Circuitry

(In the new option, the under−Voltage Protection pin does not sense the averaged value of the input voltage. Instead, a portion of the V_{in2} peak voltage is applied to the UVP pin. R18 is reduced to 1.5 kΩ that is a value better adapted to this new configuration. The voltage of the D4 and R19 common node is no more pulsating. Hence it cannot be used for synchronization. That is why R10 is now connected to V_{in1})

In addition two other modifications are performed:

- A 47 nF capacitor is placed between pin 3 (CSin+) and ground for soft−start
- The current sense capacitor C2 is increased to 12 μF (instead of 1 μF). If not, the 3.3 V rise time may be too long in full load conditions. This is because when heavily loaded, the output capacitor may charge less rapidly than the C2 one (that senses the output current) and as a consequence, the current loop may over−react further slowing down the 3.3 V rise sequence. The C2 increase does not degrade the current limitation function. Only the crossover frequency is lowered.

Doing so, very clean start−up phases are obtained as testified by the following figures. These plots were obtained in the following conditions: 10 A on the 12 V output, 10 A on the 5 V output and three different loads on the 3.3 V output: 20 A, 10 A and 0 A.

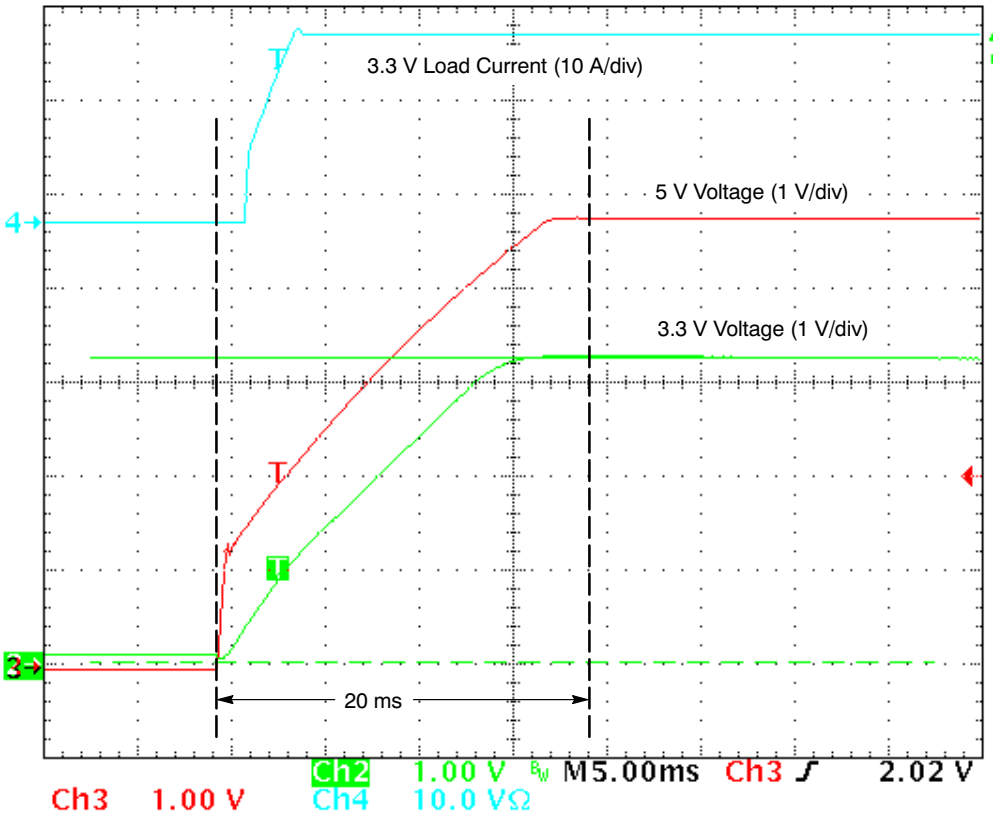


Figure 22. Start−up at Full Load (20 A on the 3.3 V Output)

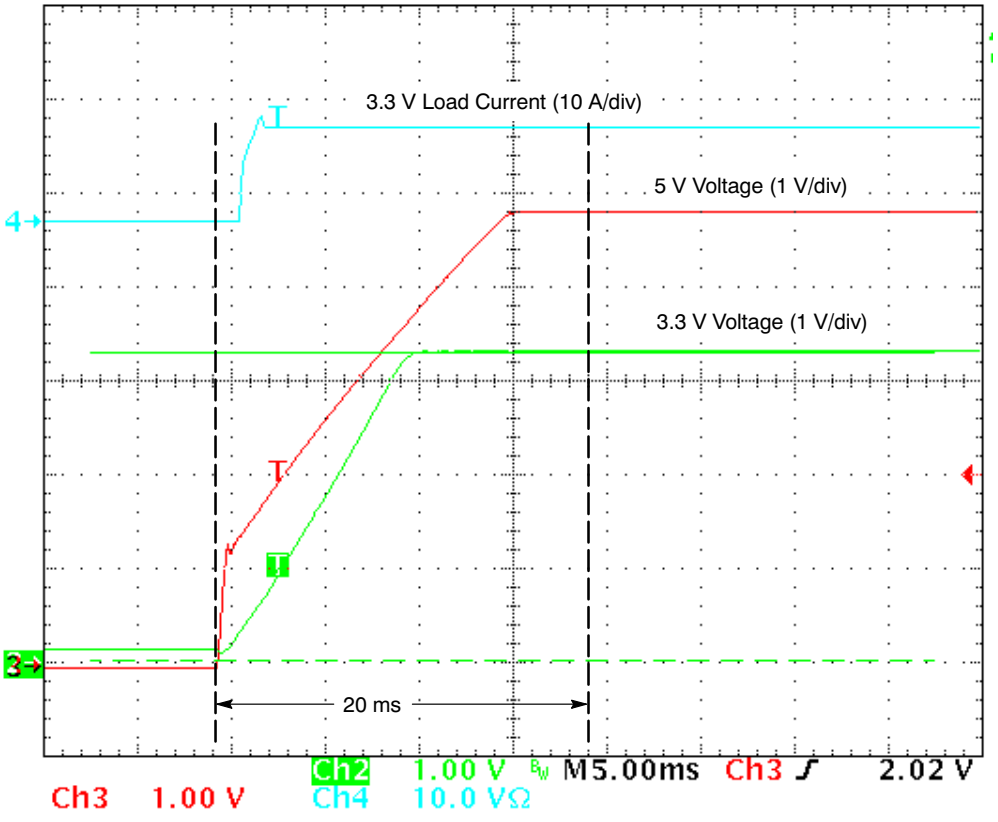


Figure 23. Start−up at Medium Load (10 A on the 3.3 V Output)

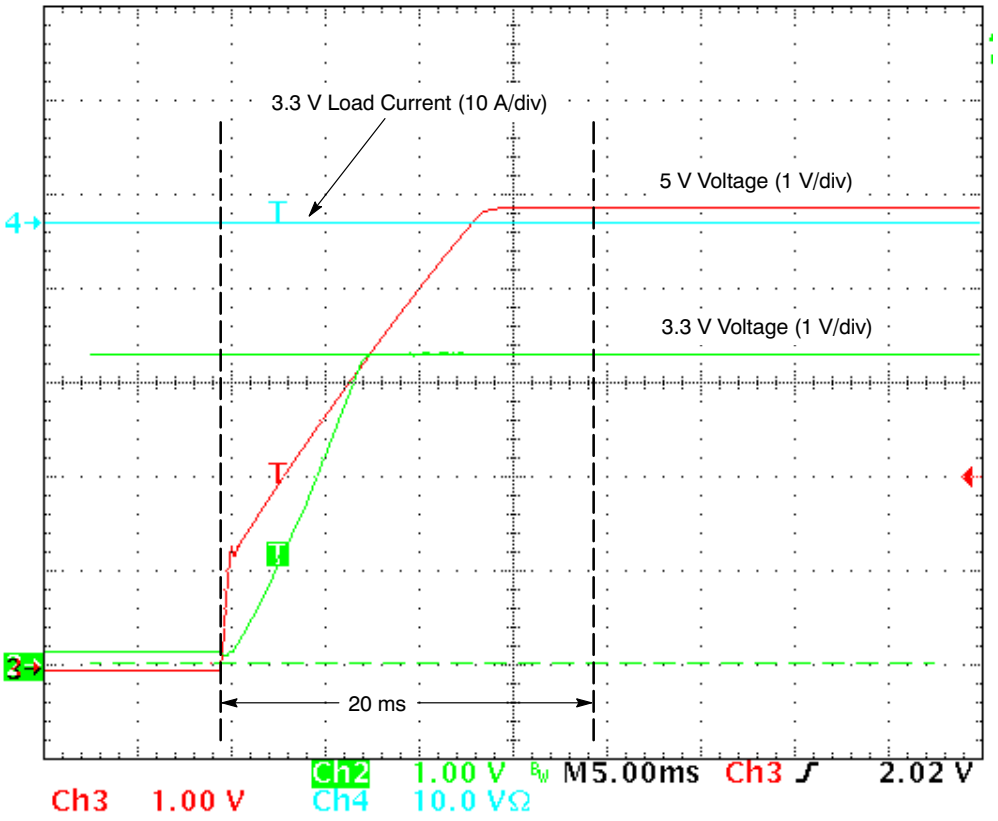


Figure 24. Start−up at No Load on the 3.3 V Output

Applications without Current Loop

In applications that do not require the use of the current loop, the following components of the application schematics can be removed: R33, R3, R32, C2, R30, R34, C15, C13 and R12 and the auxiliary operational amplifier (pins 1 to 3) can be used to control the start−up sequences.

Practically,

- a portion of the 5 V voltage is applied to pin 3 (“CSin+”). In steady state, this portion should be higher than 3.3 V not to interfere with the main voltage loop. A capacitor can be further added to soften the start−up phase (47 nF capacitor of Figure 25)
- the 3.3 V voltage is applied to pin 2 (“CSin−”) through a resistor so that the 3.3 V voltage is forced to track the portion of the 5 V voltage applied to pin 3.

The following figure sketches this tracking circuitry.

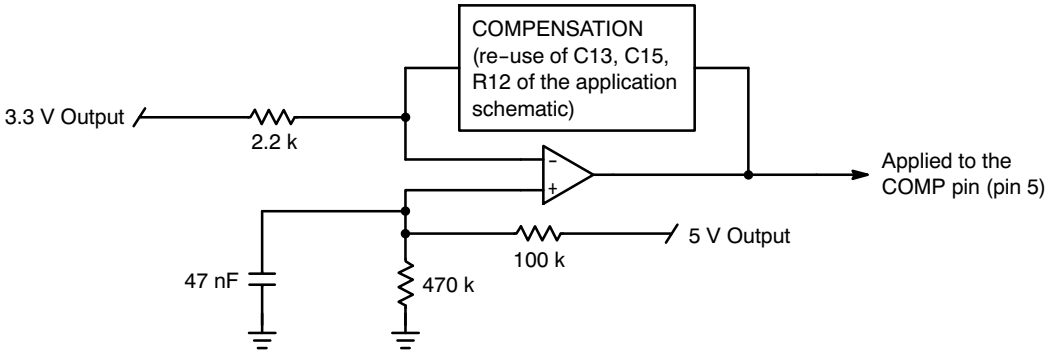


Figure 25. Tracking Circuitry

Doing so, very clean start−up phases are obtained as testified by the following figures. These plots were obtained in the following conditions: 10 A on the 12 V output, 10 A on the 5 V output and three different loads on the 3.3 V output: 20 A, 10 A and 0 A. The UVP circuitry was changed as shown by Figure 21 (peak detection instead of sensing of the averaged input voltage)

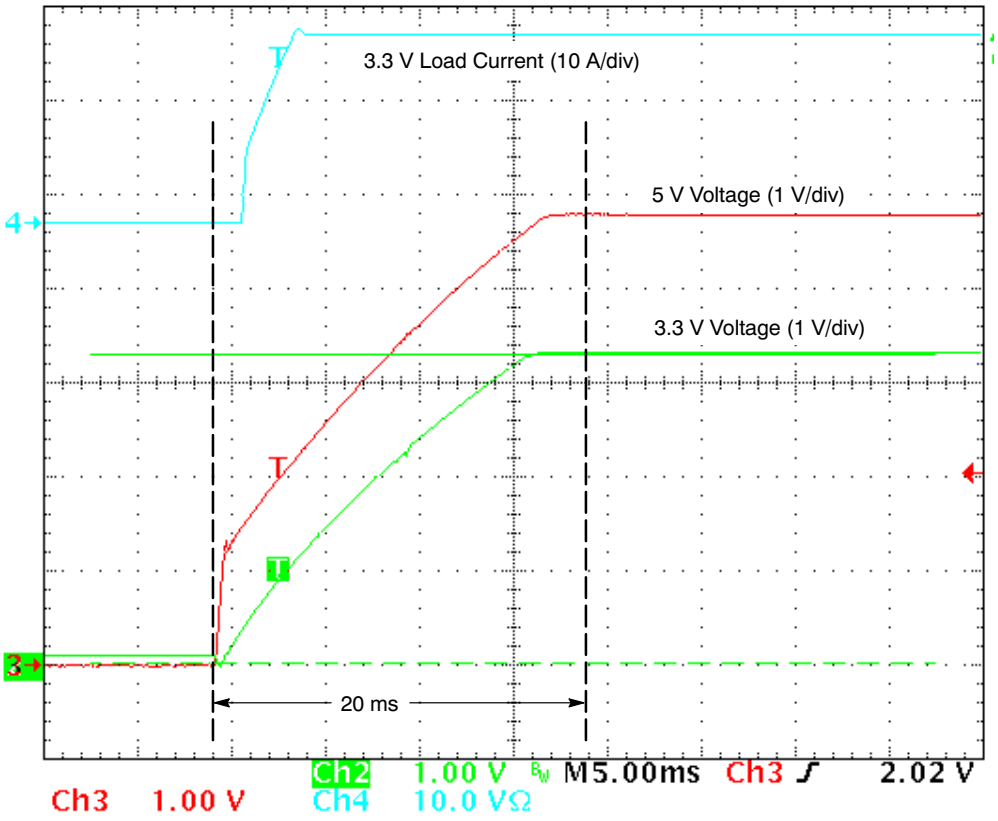


Figure 26. Start−up at Full Load (20 A on the 3.3 V Output)

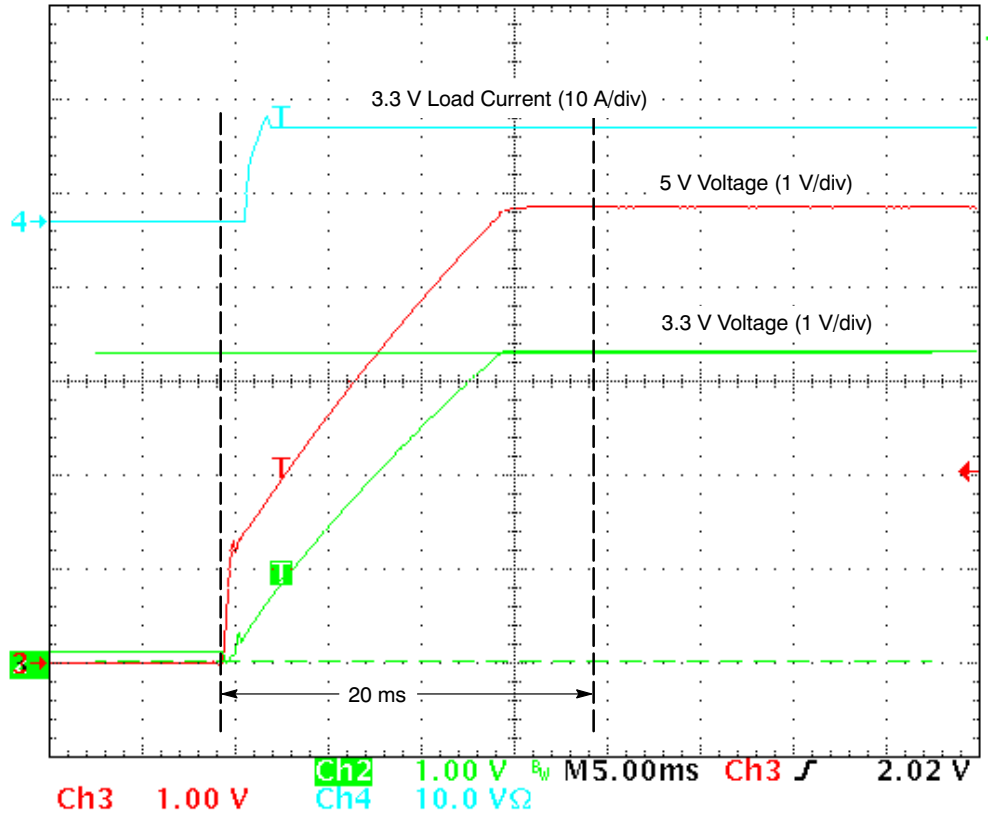


Figure 27. Start−up at Medium Load (10 A on the 3.3 V Output)

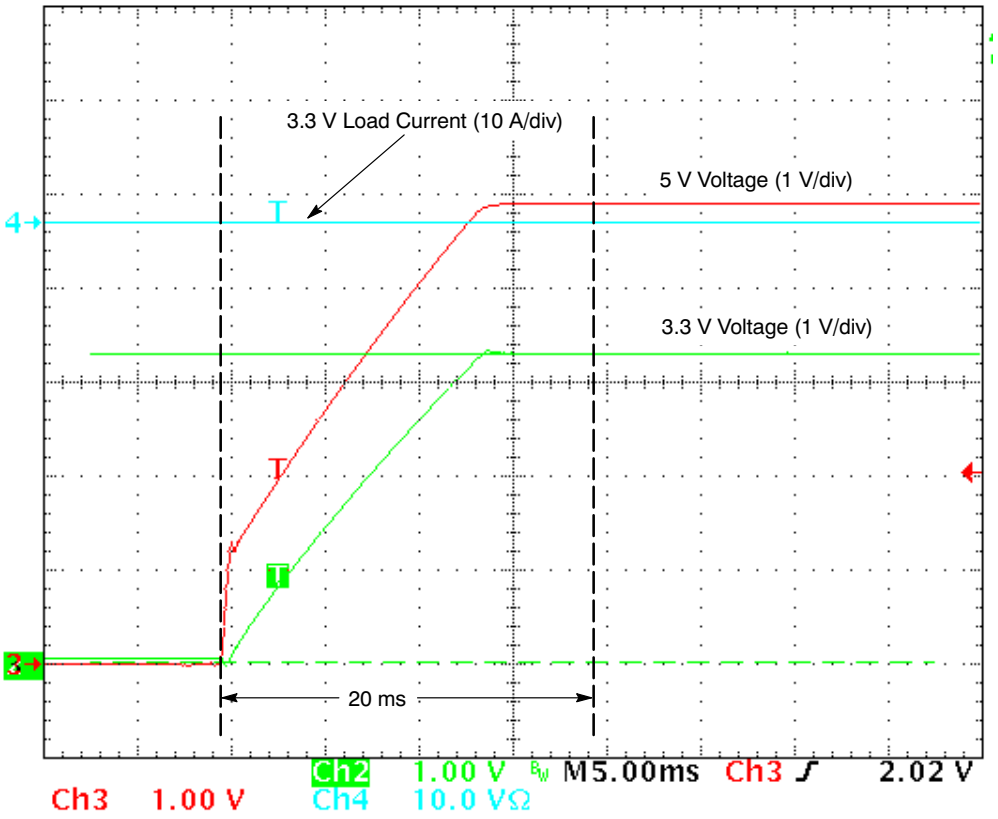


Figure 28. Start−up at No Load on the 3.3 V Output

Remark:

The described circuits to control the 3.3 V rising edges, do not degraded the stop sequences.

Let's remind that the key function in having clean stop sequences is the under−voltage protection (UVP) that must be able to detect that the main converter has stopped operating within few switching cycles. That is why C2 of Figure 21 was selected low (1 nF) not to have an excessive time constant on pin 4 (UVP pin)

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